

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

VIA HAND CARRY

This paper and the papers referred to herein as attached have been received in the U.S. Patent & Trademark Office on the date stamped below:

#2  
PATENTS

DOT. LTR  
3-5-03  
A Jones

RECEIVED  
FEB 21 2003  
TECHNOLOGY CENTER 2800

**COMBINED STATEMENT UNDER 37 C.F.R. § 3.73(b)-ESTABLISHING RIGHT OF  
ASSIGNEE TO TAKE ACTION**

**and**

**POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST (REVOCATION OF  
PRIOR POWERS)**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Sun Microsystems, Inc., a corporation organized under the laws of Delaware states that it is the assignee of entire right, title, and interest; in the patents and patent applications listed on the attached **APPENDIX A**, by virtue of an Assignment from the inventor(s) of each of the patents and patent applications listed on the attached **APPENDIX A**. Date of Recordal, and Reel and Frame number of Recordal by the United States Patent & Trademark Office identified on the attached **APPENDIX A**.

Sun Microsystems, Inc., a Delaware Corporation, having principle place of business at 901 San Antonio Road, Palo Alto, California, 94303, as assignee of record of the entire interest of the above identified patent (per above statement under 37 CFR §3.73(b)), hereby states that all powers of attorney previously given are hereby revoked.

Further, the following attorneys and/or agents are hereby appointed to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Peter B. Martine (Reg. No. 32,043)  
Albert S. Penilla (Reg. No. 39,487)  
Rick von Wohld (Reg. No. 48,018)  
Chester E. Martine, Jr. (Reg. No. 19,711)  
Lygeri Kokkinakos (Reg. No. 42,756)  
Kenneth D. Wright (Reg. No. P-53,795)

Edmund H. Mizumoto (Reg. No. 46,938)  
Joe A. Brock II (Reg. No. 46,021)  
Michael L. Gencarella (Reg. No. 44,703)  
George B. Leavell, Esq. (Reg. No. 45,436)  
Fariba Yadigar-Bandari (Reg. No. P-53,805)

provided that if any one of said attorneys ceases being affiliated with the law firm of MARTINE & PENILLA, LLP as partner or employee, such attorney's appointment as attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated; and:

Marc D. Foodman (Reg. No. 34,110)  
Timothy J. Crean (Reg. No. 37,116)  
Naren Chaganti (Reg. No. 44,602)  
Anirma R. Gupta (Reg. No. 38,275)  
Sean P. Lewis (Reg. No. 42,798)  
Michael J. Schallop (Reg. No. 44,319)  
Bernice B. Chen (Reg. No. 42,403)  
Noreen A. Krall (Reg. No. 39,734)  
Jeffrey L. Myers (Reg. No. 44,252)

Monica D. Ward (Reg. No. 40,696)  
Alexander E. Silverman (Reg. No. 37,940)  
Marilyn E. Glaubenslee (Reg. No. 35,521)  
Elaine Lee (Reg. No. 41,936)  
Hugh H. Matsubayashi (Reg. No. 43,779)  
Paul D. Sorkin (Reg. No. 39,039)  
Andrew C. Chen (Reg. No. 43,544)  
Pavel Pogodin (Reg. No. 48,205)

Of Sun Microsystems, Inc., 4120 Network Circle, MS SCA12-203, California, 95054,  
United States of America.

**Please send all correspondence to:**

**Albert S. Penilla, Esq.**  
**MARTINE & PENILLA, LLP**  
710 Lakeway Dr., Suite 170  
Sunnyvale, CA 94085  
**Customer Number 25,920**

**Please direct telephone calls to:**

**Albert S. Penilla, Esq. at (408) 749-6903.**

The undersigned is authorized to act on behalf of the Assignee.

Marilyn E. Glaubenslee 12/13/02  
(Signature of authorized person) (date)

Marilyn E. Glaubenslee  
(type or print name of authorized person)  
Assistant General Counsel, having delegated Power  
to sign on Behalf of Sun Microsystems, Inc.

Title of authorized person

Appendix A  
Page 1 of 4

Serial Number	Filing Date	Patent	Date Issued or Abandoned	Status	Reel And Frame	Title	Client Number	Case Number
64,655	5/28/1997	5,966,537	10/12/1999	Issued	8576/0857	METHOD AND APPARATUS FOR DYNAMICALLY OPTIMIZING AN EXECUTABLE COMPUTER PROGRAM USING INPUT DATA	P2017/MG	SUNMP246
08/884,255	6/27/1997	6,088,786	6/11/2000	Issued		METHOD AND SYSTEM FOR COUPLING A STACK BASED PROCESSOR TO REGISTER BASED FUNCTIONAL UNIT	P2107/MG	SUNMP247
						METHOD AND APPARATUS FOR CONVERTING EXECUTABLE COMPUTER PROGRAMS IN A HETEROGENEOUS COMPUTING ENVIRONMENT		
08/865,335	5/28/1997	6,035,120	3/7/2000	Issued	8599/0415	METHOD AND APPARATUS FOR GENERATING AN OPTIMIZED TARGET EXECUTABLE COMPUTER PROGRAM USING AN OPTIMIZED SOURCE EXECUTABLE	P2132/MG	SUNMP248
08/864,247	5/28/1997	5,966,536	10/12/1999	Issued	8582/0110	MODULAR COPROCESSOR UNIT WITH INTEGRATED MULTIMEDIA FUNCTIONS	P2134/MG	SUNMP249
09/364,926	7/26/1999		3/23/2001	Abandoned		PROCESSOR COUPLED BY VISIBLE REGISTER SET TO MODULAR COPROCESSOR INCLUDING INTEGRATED MULTIMEDIA UNIT	P2258/MG	SUNMP250
09/687,608	10/12/2000	6,334,180	12/25/2001	Issued		METHOD FOR SCAN TEST OF SRAM FOR MICROPROCESSORS HAVING FULL SCAN CAPABILITY	P2258CNT1/MG	SUNMP250C
08/880,468	6/23/1997	5,923,835	7/13/1999	Issued	8832/0598	BRANCH INSTRUCTION PREDICTION APPARATUS	P2271/MG	SUNMP251
08/881,798	6/24/1997	5,857,098	1/5/1999	Issued	010719/0771	METHOD FOR INCREMENTAL TIMING OF AN INTEGRATED CIRCUIT	P2508/MG	SUNMP253
09/076,319	5/11/1998		10/30/2000	Abandoned			P2788/MG	SUNMP254

Appendix A  
Page 2 of 4

Serial Number	Filing Date	Patent	Date Issued or Abandoned	Status	Reel And Frame	Title	Client Number	Case Number
09/021,969	2/11/1998	6,128,636	10/3/2000	Issued	9884/0245	METHOD FOR INTERFACING FLOATING POINT AND INTERGER PROCESSES IN A COMPUTER SYSTEM	P2794/MG	SUNMP255
09/089,626	6/1/1998	6,263,399	7/17/2001	Issued	9403/0348	MICROPROCESSOR TO NAND FLASH INTERFACE	P2858/MG	SUNMP257
09/121,025	7/22/1998	6,092,125	7/18/2000	Issued	010707/0750	METHOD AND APPARATUS FOR TRANSFERRING DATA FROM DEVICES NOT SUPPORTING BURST DATA TRANSFERS IN BURST MODE	P2863/MG	SUNMP258
09/139,956	8/25/1998	6,104,215	8/15/2000	Issued	9694/0184	SIGNAL DETECTOR WITH IMPROVED NOISE IMMUNITY	P2910/MG	SUNMP259
09/239,903	11/29/2003	6,212,594	4/3/2001	Issued	010131/0752	TIMER WITH FIXED AND PROGRAMMABLE INTERRUPT PERIODS	P3069/MG	SUNMP260
08/881,103	6/24/1997			Abandoned		MECHANISM FOR ENSURING CONSISTENCY OF INSTRUCTION CACHE	P2505/MG	SUNMP262
09/320,240	5/26/1999			Pending	010168/0628	PERIPHERAL CORE BUMPS FOR INTEGRATED CIRCUITS	P3458/MG	SUNMP266
90,071	9/3/1999			Pending	010244/0282	QUOTIENT DIGIT SELECTION LOGIC FOR FLOATING POINT DIVISION/SQUARE ROOT	P3657/MG	SUNMP269
09/511,218	2/23/2000			Pending	010590/0484	OPTIMIZED SYSTEM AND METHOD FOR PARALLEL LEADING ONE/ZERO ANTICIPATION	P4006/MG	SUNMP276
09/436,464	11/8/1999			Pending	010507/0041	METHOD AND APPARATUS FOR INSERTING DATA PREFETCH OPERATIONS USING DATA FLOW ANALYSIS	P4373/MG	SUNMP282
09/632,235	8/4/2000			Pending	011226/0495	ELIMINATION OF END-AROUND-CARRY CRITICAL PATH IN FLOATING POINT ADD/SUBTRACT EXECUTION UNIT	P4497/MG	SUNMP285

Appendix A  
Page 3 of 4

Serial Number	Filing Date	Patent	Date Issued or Abandoned	Status	Reel And Frame	Title	Client Number	Case Number
09/564,202	5/3/2000			Pending	010789/0767	ACTIVE ADDRESS CONTENT ADDRESSABLE MEMORY	P4509/MG	SUNMP287
09/501,549	2/9/2000			Pending	010552/0568	SYSTEM AND METHOD FOR FINE-GRAINED ANALYSIS OF COMPLEX SOFTWARE	P4508/MG	SUNMP288
09/513,662	2/25/2000			Pending		REINSTATE APPARATUS AND METHOD TO RECREATE DATA BACKGROUND FOR TESTING SRAM	P4555/MG	SUNMP289
09/625,522	7/26/2000			Pending	010973/0398	MULTIPLEXER SELECT LINE EXCLUSIVITY CHECK METHOD AND APPARATUS	P4659/MG	SUNMP291
09/590,786	6/8/2000			Pending	010857/0606	SYSTEM AND METHOD FOR IMPLEMENTING MEMORY TESTING IN A SRAM UNIT	P4656/MG	SUNMP292
09/614,418	7/12/2000			Pending	010938/0828	READ CONTROL SYSTEM AND METHOD FOR TESTING WORD ORIENTED SRAM WITH MACROS	P4657/MG	SUNMP293
09/535,930	3/24/2000			Pending	010647/0907	MODULO SCHEDULING VIA BINARY SEARCH FOR MINIMUM ACCEPTABLE INITIATION INTERVAL METHOD AND APPARATUS	P4678/MG	SUNMP294
09/586,657	6/1/2000			Pending	010842/0163	PARALLEL GREATER THAN ANALYSIS METHOD AND APPARATUS	P4891/MG	SUNMP295
09/586,658	6/1/2000			Pending		OPTIMIZED METHOD AND APPARATUS FOR PARALLEL LEADING ZERO/ONE DETECTION	P5097/MG	SUNMP300
09/679,945	10/4/2000			Pending	011207/0502	USING VALUE-EXPRESSION GRAPHS FOR DATA-FLOW OPTIMIZATIONS	P5333/MG	SUNMP301
09/823,207	3/30/2001			Pending	011680/0581	METHOD AND APPARATUS FOR SIMULTANEOUS OPTIMIZATION OF CODE TARGETING MULTIPLE MACHINES	P5446/MG	SUNMP303

Appendix A  
Page 4 of 4

Serial Number	Filing Date	Patent	Date Issued or Abandoned	Status	Reel And Frame	Title	Client Number	Case Number
09/872,065	5/31/2001			Pending	011876/0023	METHOD AND SYSTEM FOR PROVIDING A HEURISTIC APPROACH FOR TESTING CELL LIBRARIES	P5472/MG	SUNMP304
10/072,234	2/6/2002			Pending	012941/0774	METHOD AND SYSTEM FOR PROVIDING A SECURED WIDE AREA NETWORK ACCESS	P5554/MG	SUNMP307
10/082,430	2/22/2002			Pending	012642/0519	INTEGRATED ELECTROMIGRATION LENGTH EFFECT TESTING METHOD AND APPARATUS	P6557/MG	SUNMP308
09/996,339	3/21/2002			Allowed	012649/0639	FULLY INTEGRATED COMPUTER RACKING SYSTEM	P6581/MG	SUNMP309